ANALYSIS OF SINGLE PHASE MLI FOR GRID CONNECTED PV SYSTEM

Niharika Jain[1], Santosh Kumar[2]
E-Mail Id: jainniharika.jain@gmail.com[1], santosh_en@rediffmail.com[2]
Department of Electrical & Electronics Engineering, Millennium Institute of Technology & Science, Bhopal (MP), India

Abstract- This paper present a single phase seven level photovoltaic (PV) inverter topology for grid connected PV system with a novel Pulse Width Modulation (PWM) control scheme. Three reference signals identical to each other with an offset equivalent to the amplitude of the triangular carrier signal were used to generate PWM signals for the switch. A Proportional Integral Derivative (PID) current control algorithm is implemented.to keep the current injected into the grid sinusoidal and to have high dynamic performance with rapidly changing atmospheric conditions. The inverter offers much less total harmonics distortion and can operate at near-unity power factor. Simulation results are compared with the conventional single phase three level and five level grid connected PWM inverter. The inverter is capable of producing seven level of output-voltage levels V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$ from the DC supply voltage. Simulation results have been presented to demonstrate the suitability of the control method. Simulation results exhibits improved performance of the system.
Keywords - Grid Connected, MLI, PV, PWM, THD, MATLAB/ SIMULINK.

1. INTRODUCTION

The ever-increasing energy consumption, fossil fuels' soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [3]. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [3], [4]. Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped [5] – [10], flying capacitor or multi cell [11]–[17], cascaded H-bridge [18]–[24], and modified H-bridge multilevel [25]–[29]. This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

2. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed single-phase seven-level inverter was developed from the five-level inverter in. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C1, C2, and C3, as shown in fig. 2.1.

The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitors for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance L_f was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$) from the dc supply voltage. The proposed inverter's operation can be divided into seven switching states, as shown in Fig 2.2 (a) to Fig. 2.2 (g). Fig. 2.2 (a), (d), and (g) shows a conventional inverter's operational states in sequence, while Fig 2.2 (b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one and two-third levels of the dc-bus voltage.

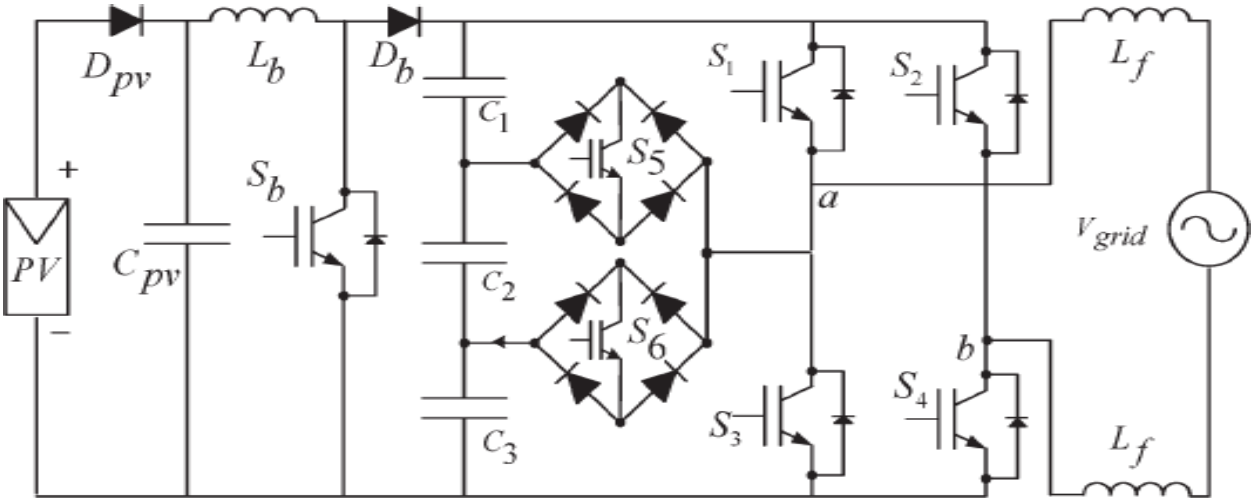

Fig. 2.1 Proposed Inverter Topology

The required seven levels of output voltage were generated as follows

- Maximum Positive Output (V_{dc}): S1 is ON, connecting the load positive terminal to V_{dc}, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc}. Fig. 2.2 (a) shows the current paths that are active at this stage.
- Two-Third Positive Output ($2V_{dc}/3$): The bidirectional switch S5 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $2V_{dc}/3$. Fig. 2.2 (b) shows the current paths that are active at this stage.
- One-Third Positive Output ($V_{dc}/3$): The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}/3$. Fig. 2.2 (c) shows the current paths that are active at this stage.
- Zero Output (0): This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 and S2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and the voltage applied to the load terminals is zero. Fig. 2.2 (d) shows the current paths that are active at this stage.

- One-Third Negative Output ($-V_{dc}/3$): The bidirectional switch S5 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to V_{dc}. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}/3$. Fig. 2.2 (e) shows the current paths that are active at this stage.
- Two-Third Negative Output ($-2V_{dc}/3$): The bidirectional switch S6 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-2V_{dc}/3$. Fig. 2.2 (f) shows the current paths that are active at this stage.
- Maximum Negative Output ($-V_{dc}$): S2 is ON, connecting the load negative terminal to V_{dc}, and S3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}$. Fig. 2.2 (g) shows the current paths that are active at this stage.

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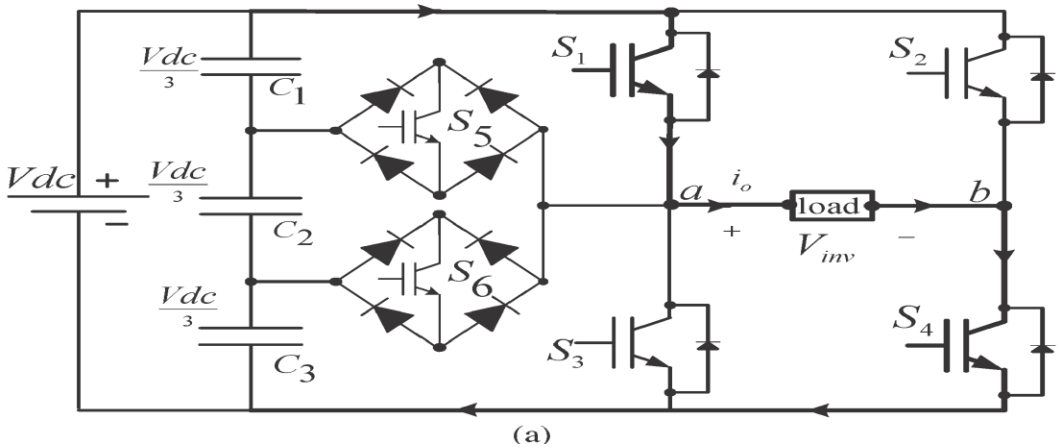
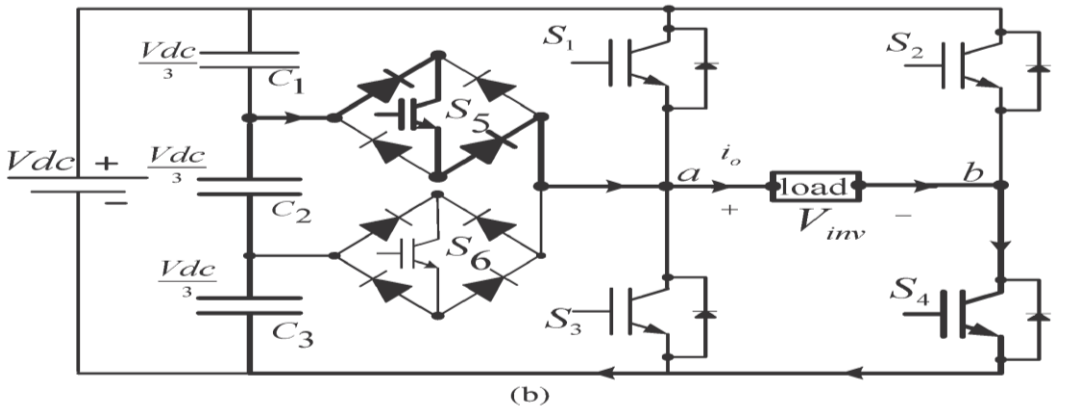
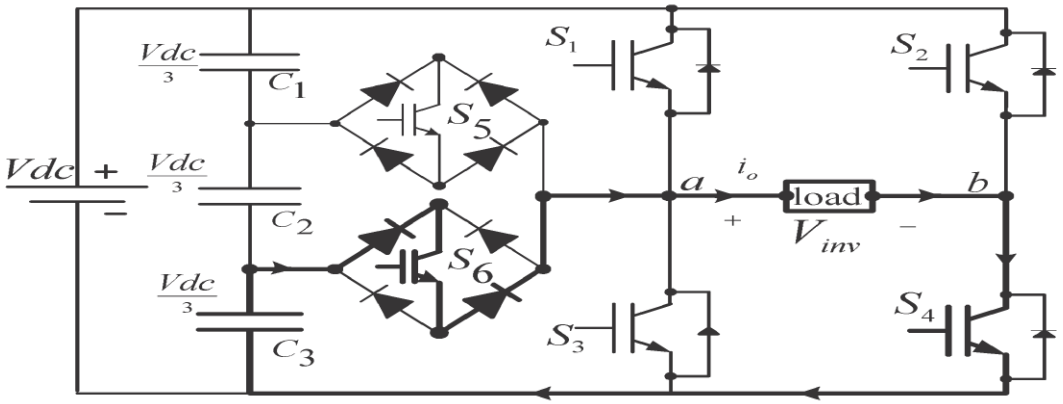


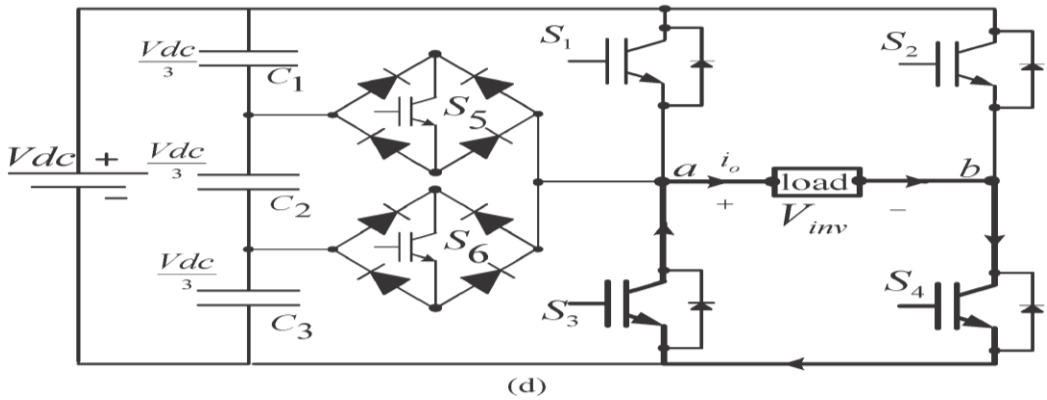
(a)



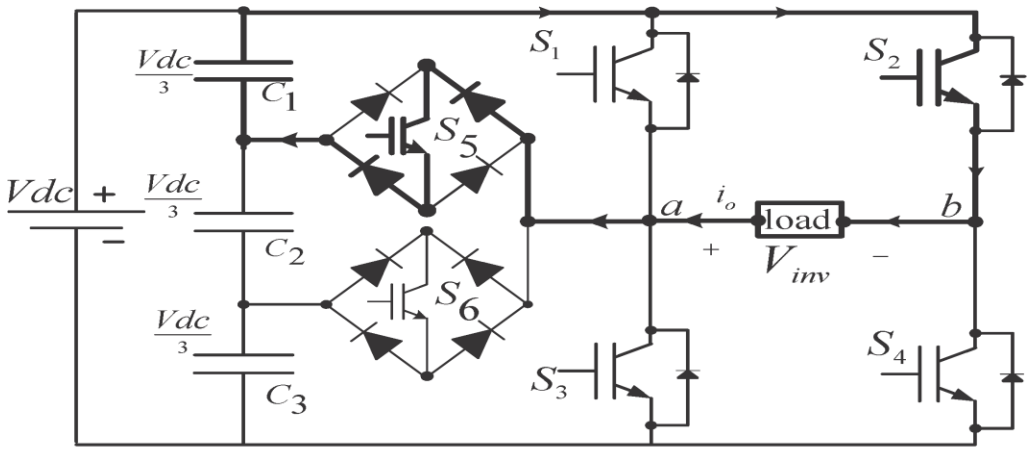
(b)



(c)



(d)



(e)

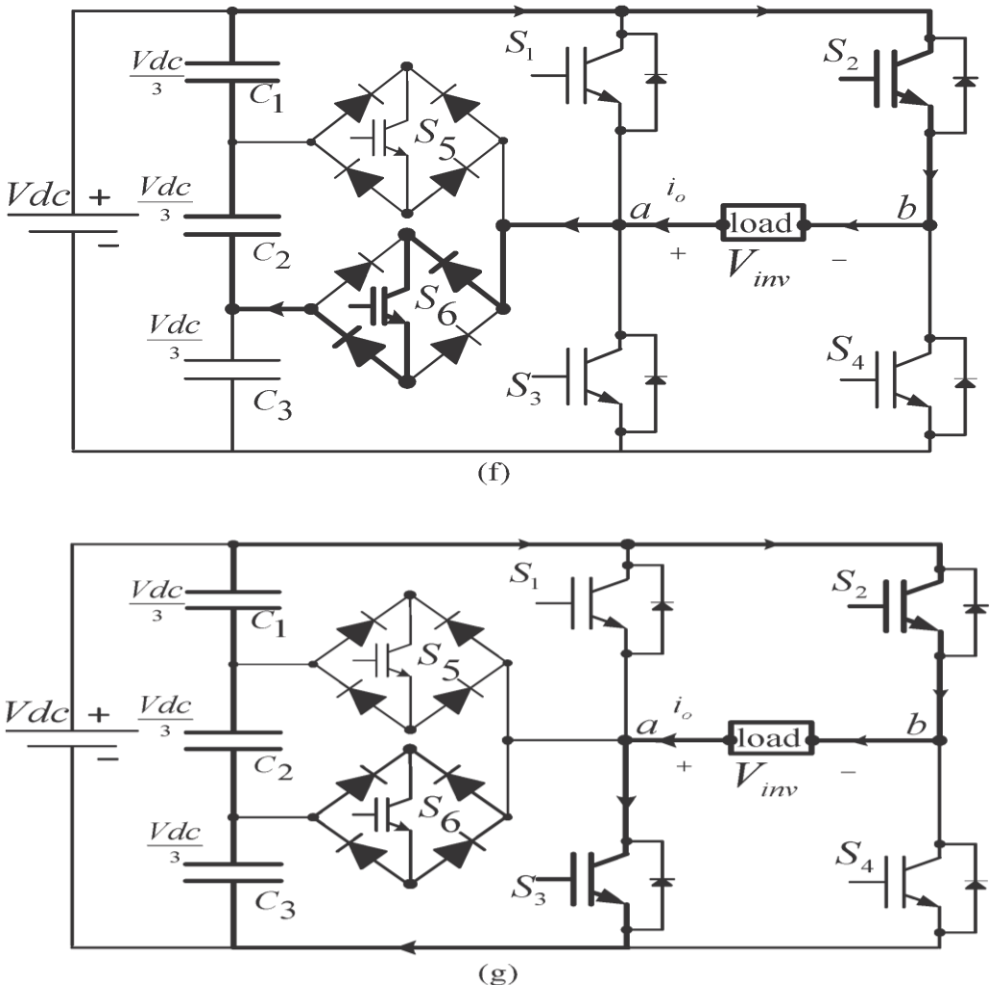


Fig. 2.2 Switching Combination Required to Generate the Output Voltage (V_{ab}). (A) $V_{ab} = V_{dc}$. (B) $V_{ab} = 2V_{dc}/3$. (C) $V_{ab} = V_{dc}/3$. (D) $V_{ab} = 0$ (E) $V_{ab} = -V_{dc}/3$. (F) $V_{ab} = -2V_{dc}/3$. (G) $V_{ab} = -V_{dc}$

Table: 1 illustrates the level of voltage during S1–S6 switch on and off. This table also shows the output voltage according to the switches' On-Off condition

Table-2.1 Output Voltage According to the Switches ON (1) – OFF (0) Condition

Vo	S1	S2	S3	S4	S5	S6
V_{dc},	1	0	0	1	0	0
$2V_{dc}/3$	0	0	0	1	1	0
$V_{dc}/3$	0	0	0	1	0	1
0	0	0	1	1	0	0
0*	1	1	0	0	0	0
$-V_{dc}$	0	1	0	0	1	0
$-2V_{dc}/3$	0	1	0	0	0	1
$-V_{dc}/3$	0	1	1	0	0	1

3. PWM MODULATION

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals V_{ref1}, V_{ref2} and V_{ref3} will take turns to be compared with the carrier signal at a time. Figure 3.1 shows the carrier and reference signals. If V_{ref1} had exceeded the peak amplitude of $V_{carrier}$, V_{ref2} was compared with $V_{carrier}$ until it had exceeded the peak amplitude of $V_{carrier}$. Then, onward, V_{ref3} would take charge and would be compared with $V_{carrier}$ until it reached zero. Once V_{ref3} had reached zero, V_{ref2} would be compared until it reached zero. Then, onward, V_{ref1} would be compared with $V_{carrier}$. Fig. 3.2 shows the resulting switching pattern. Switches S1, S3, S5,

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Paper Id: IJTRS-ES-004

and S6 would be switching at the rate of the carrier signal frequency, whereas S2 and S4 would operate at a frequency that was equivalent to the fundamental frequency.

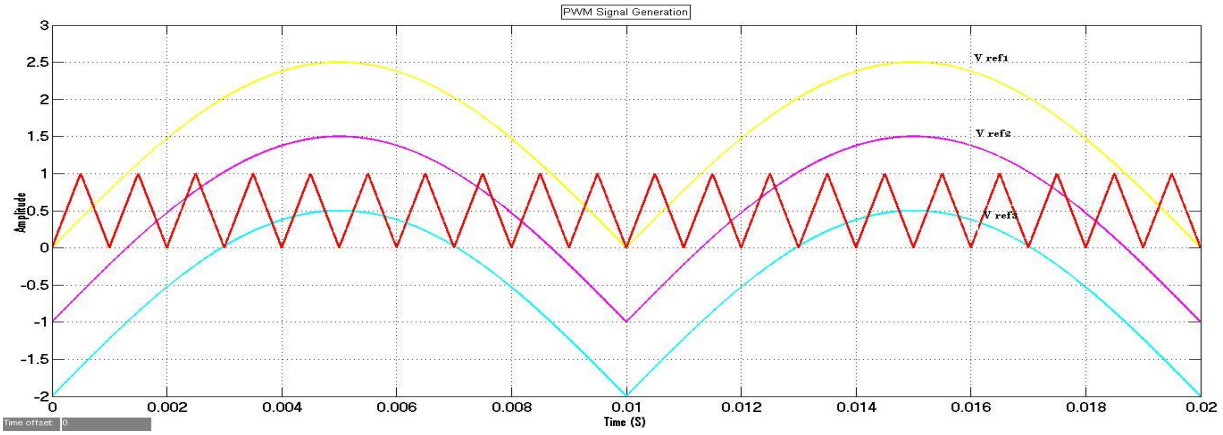

Fig. 3.1 Reference and Carrier Signals

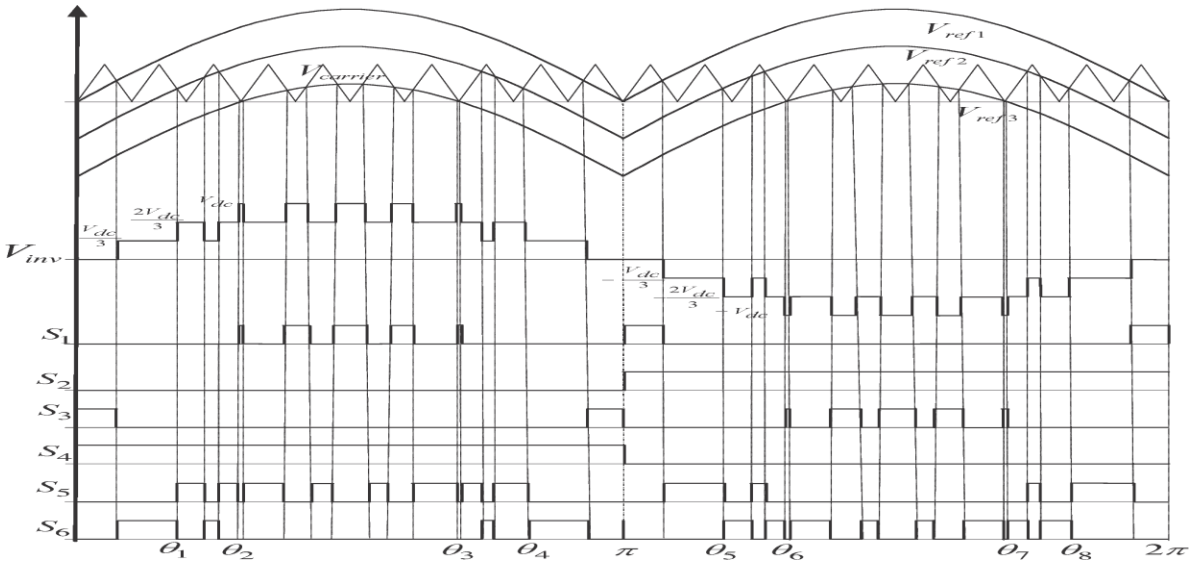

Fig. 3.2 Switching Pattern for the Single-Phase Seven-Level Inverter

For one cycle of the fundamental frequency, the proposed inverter operated through six modes. Fig. 3.3 shows the per unit output-voltage signal for one cycle. The six modes are described as follows:

Mode 1: $0< \omega t < \theta_1$ and $\theta 4 < \omega t < \pi$

Mode 2: $\theta_1 < \omega t < \theta_2$ and $\theta_3 < \omega t < \theta_4$

Mode 3: $\theta_2 < \omega t < \theta_3$

Mode 4: $\pi < \omega t < \theta_5$ and $\theta_8 < \omega t < 2\pi$

Mode 5: $\theta_5 < \omega t < \theta_6$ and $\theta_7 < \omega t < \theta_8$

Mode 6: $\theta_6 < \omega t < \theta_7$.

The phase angle depends on modulation index Ma. Theoretically, for a single reference signal and a single carrier signal, the modulation index is defined to be

$$M_a = \frac{A_m}{A_c}$$

While for a single-reference signal and a dual carrier signal, the modulation index is defined to be [26]–[29]

$$M_a = \frac{A_m}{2A_c}$$

Since the proposed seven-level PWM inverter utilizes three carrier signals, the modulation index is defined to be

$$M_a = \frac{A_m}{3A_c}$$

Where Ac is the peak-to-peak value of the carrier signal and Am is the peak value of the voltage reference signal V_{ref}.

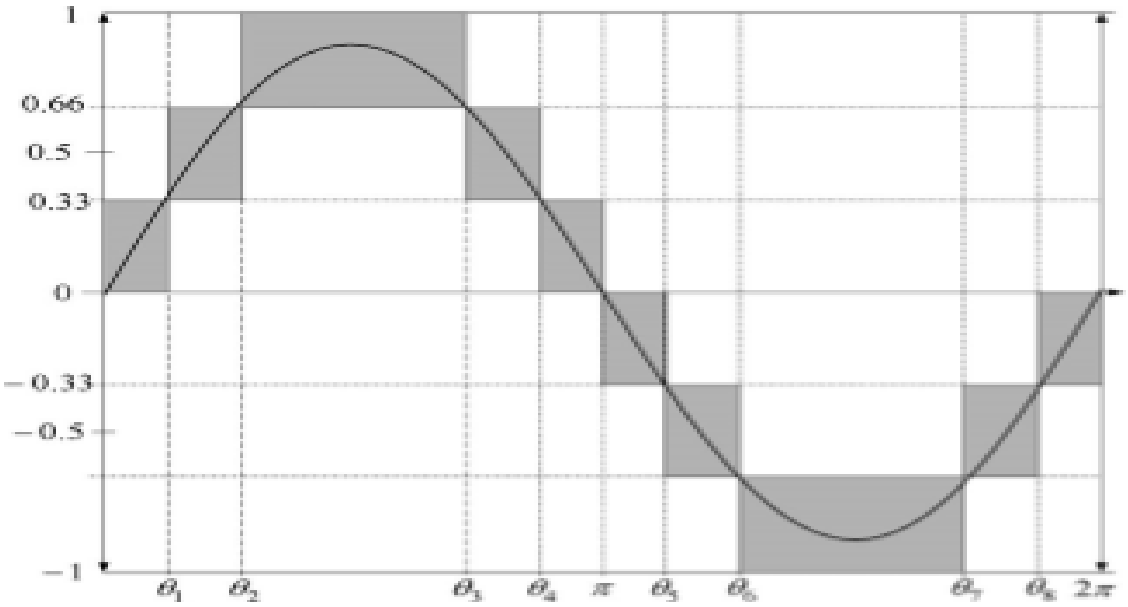

Fig. 3.3 Seven-Level Output Voltage (Vab) and Switching Angles

When the modulation index is less than 0.33, the phase angle displacement is

$\theta_1 = \theta_2 = \theta_3 = \theta_4 = \pi/2$

$\theta_5 = \theta_6 = \theta_7 = \theta_8 = 3\pi/2$

On the other hand, when the modulation index is more than 0.33 and less than 0.66, the phase angle displacement is determined by

$$\theta_1 = \sin^{-1}\left(\frac{A_c}{A_m}\right)$$

$\theta_2 = \theta_3 = \pi/2$

$\theta_4 = \pi - \theta_1$

$\theta_5 = \pi + \theta_1$

$\theta_6 = \theta_7 = 3\pi / 2$

$\theta_8 = 2\pi - \theta_1$

If the modulation index is more than 0.66, the phase angle displacement is determined by

$$\theta_1 = \sin^{-1}\left(\frac{A_c}{A_m}\right)$$

$$\theta_2 = \sin^{-1}\left(\frac{2A_c}{A_m}\right)$$

$\theta_3 = \pi - \theta_2$

$\theta_4 = \pi - \theta_1$

$\theta_5 = \pi + \theta_1$

$\theta_6 = \pi + \theta_2$

$\theta_7 = 2\pi - \theta_2$

$\theta_8 = 2\pi - \theta_1$

For Ma that is equal to, or less than, 0.33, only the lower reference wave (V_{ref3}) is compared with the triangular carrier signal. The inverter's behavior is similar to that of a conventional full-bridge three-level PWM inverter. However, if Ma is more than 0.33 and less than 0.66, only V_{ref2} and V_{ref3} reference signals are compared with the triangular carrier wave. The output voltage consists of five dc-voltage levels. The modulation index is set to be more than 0.66 for seven levels of output voltage to be produced. Three reference signals have to be compared with the triangular carrier signal to produce switching signals for the switches.

4. SIMULATION MODEL & RESULT ANALYSIS

A simulation in MATLAB/Simulink utilizing Sim Power System was conducted to investigate the effectiveness of the developed single phase seven level inverter for grid connected PV system. It was simulated for 0.045 seconds with a sampling period of 1 μs. The simulation modeling is shown in figure 4.1.

DOI Number: https://doi.org/10.30780/specialissue-electrical system/004 pg. 30
Paper Id: IJTRS-ES-004

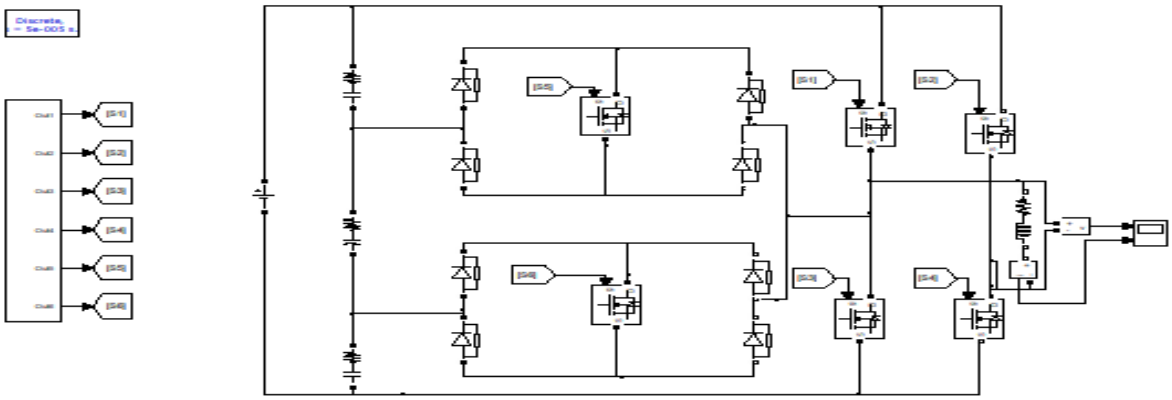

Fig. 4.1 Simulation Model of Single Phase Seven Level Inverter for Grid Connected PV System

MAT LAB SIMULINK simulated the proposed configuration before it was physically implemented. The PWM switching patterns were generated by comparing three reference signals (V_{ref1}, V_{ref2}, and V_{ref3}) against a triangular carrier signal as shown in figure 4.2.

Subsequently, the comparing process produced PWM switching signals for switches S1–S6, as shown in figure 4.3. One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (50 Hz). Switches S5 and S6 also operated at the rate of the carrier signal. Fig. 4.4 shows the simulation result of inverter output voltage (V). Fig. 4.6 shows the simulation result of inverter output current (A).

Table 4.1 shows the value of simulation parameters used during the simulation work, Table 4.2 shows the comparative THD analysis of multilevel inverter and fig. 4.7 show the FFT analysis of single phase seven level inverter.

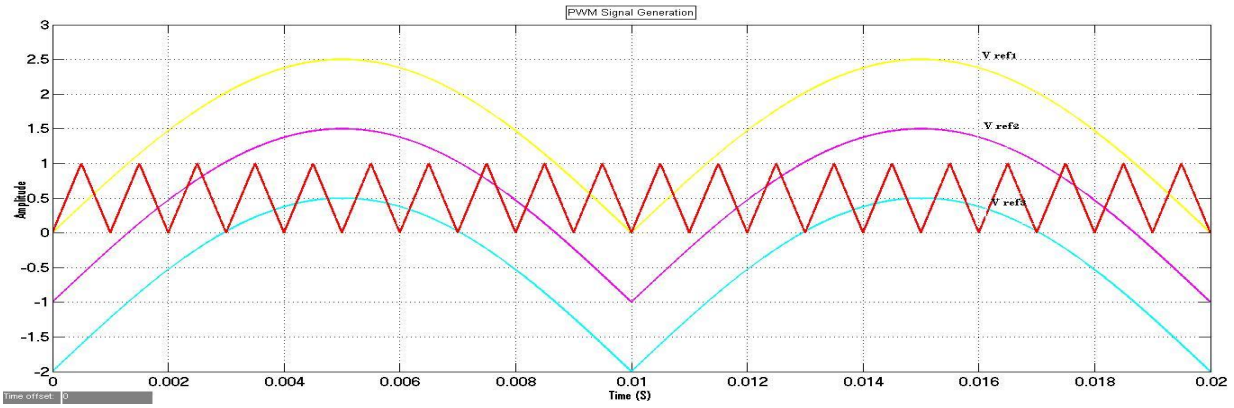

Fig. 4.2 PWM Switching Signal Generation

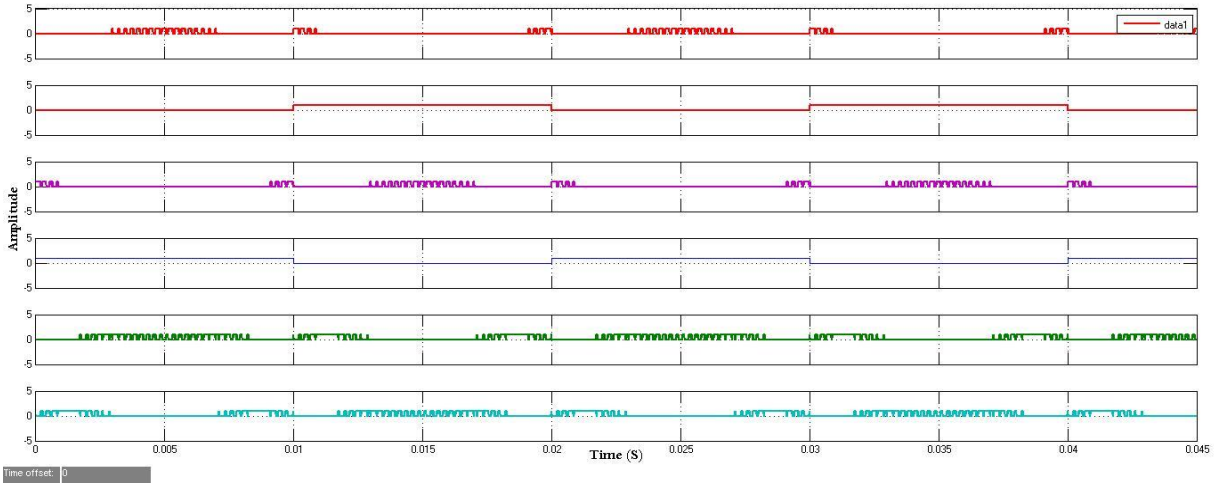

Fig. 4.3 PWM Signals for Switches S1-S6

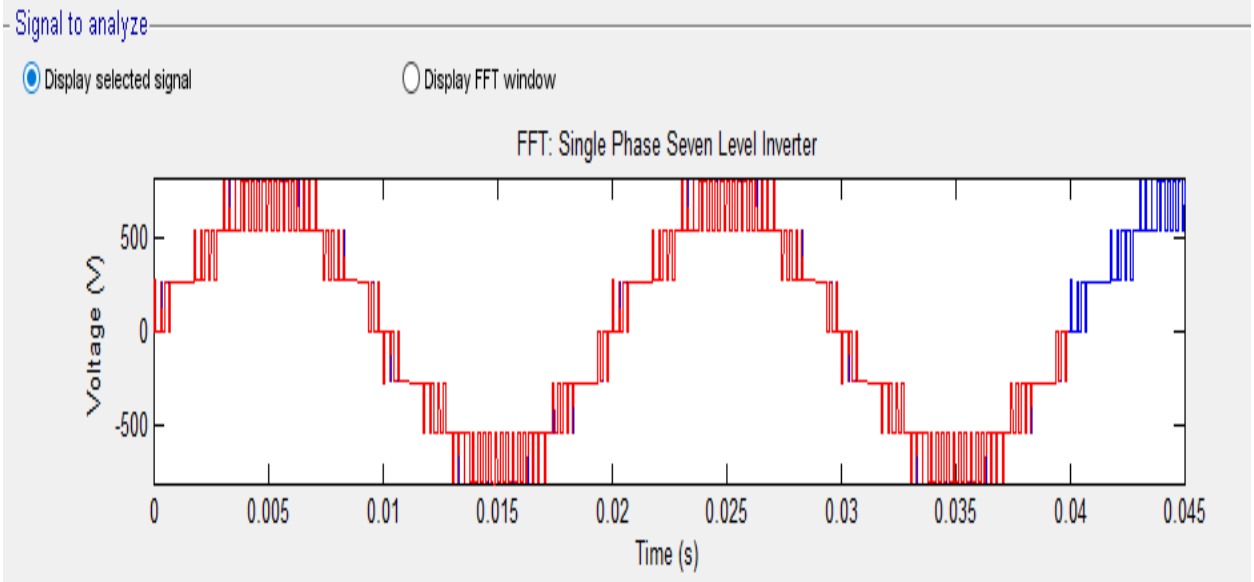

Fig. 4.4 Inverter Output Voltage

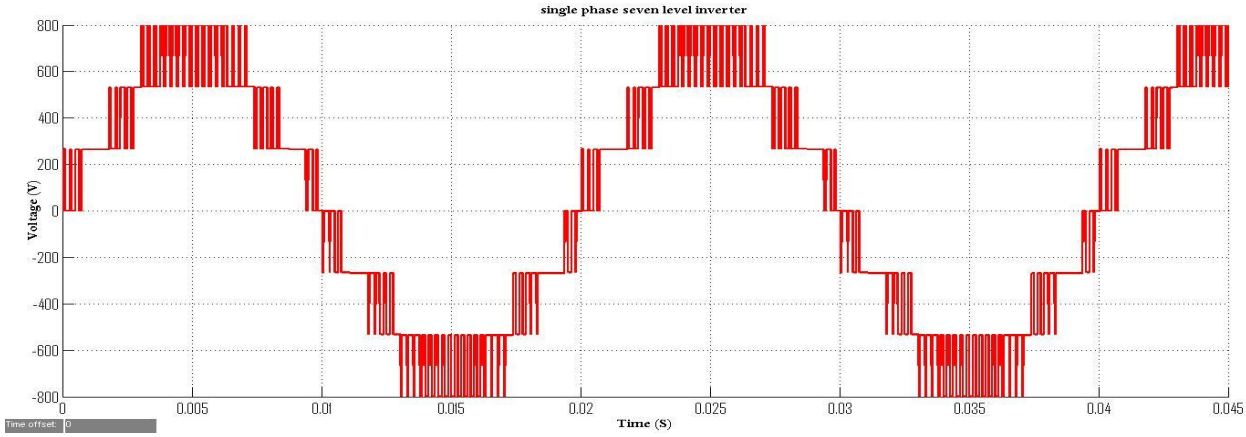

Fig. 4.5 Inverter Output Current

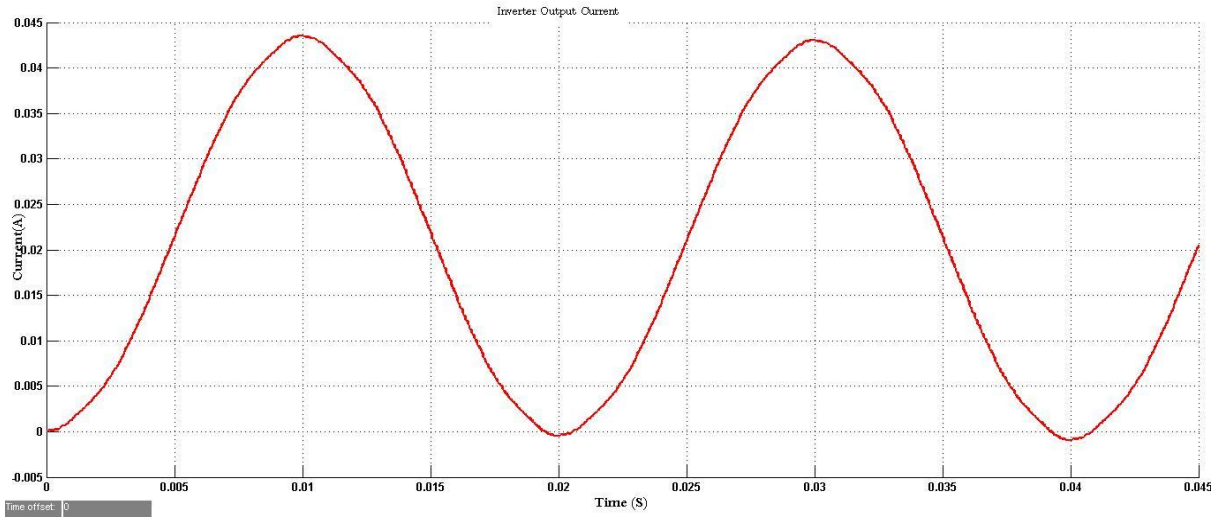

Fig. 4.6 FFT Analysis of Single Phase Seven Level Inverter Output Voltage

DOI Number: https://doi.org/10.30780/specialissue-electrical system/004 **pg. 32**
Paper Id: IJTRS-ES-004

Table-4.1 Simulation Parameters

S. No	Parameter	Value
1	DC Input Voltage	800 V
2	DC Link Capacitance	2200 μF
3	Load Resistance	100 Ω
4	Load Inductance	100 H
5	AC Output Voltage	800 V
6	AC Output Current	0.045 A
7	Switching Frequency	2 KHz

Table-4.2 THD Analysis of Multi-Level Inverters

S. No	Multi-Level Inverter	THD (%)
1	Thee Level	8.0 %
2	Five Level	5.4 %
3	Seven Level	3.9 %
4	Proposed Seven Level	1.51 %

The simulation results are presented to validate the effectiveness of the developed inverter control system algorithm. In addition, to assess the capability of the developed system protection, the disturbances in grid voltage and frequency are introduced. The disturbances are over voltage, under voltage, over frequency and under frequency. For grid-connected mode, the injected current must be nearly sinusoidal with a unity power factor and 1.51 % of total harmonic distortion (THD).

CONCLUSIONS

The simulation results are presented to validate the effectiveness of the developed inverter control system algorithm. In addition, to assess the capability of the developed system protection, the disturbances in grid voltage and frequency are introduced. The disturbances are over voltage, under voltage, over frequency and under frequency. For grid-connected mode, the injected current must be nearly sinusoidal with a unity power factor and 1.51 % of total harmonic distortion (THD). The less THD in the seven-level inverter compared with that in the five and three-level inverters is an attractive solution for grid-connected PV inverters. The THD in the proposed seven-level inverter compared with that in the seven-level inverter, five level inverters and three-level inverters is 1.51%, 3.9%, 5.4% and 8.0% respectively. The presented results showed that the inverter control algorithm is successful in converting PV dc power to ac power with acceptable THD level for supplying power to the load and grid as well. In addition, the system manages to regulate the 50Hz sinusoidal output voltage and response to the grid voltage and frequency disturbances effectively. Overall, this investigation has proved the good performance of the developed inverter control system algorithm.

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